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A New Single-Switch Bridgeless PFC Dual-Output-Polarities Converter with Series-Line-Diode-Clamped Configuration for Elimination Circulating Current and Capacitive Coupling Loop

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ABSTRACT

This paper presents a new single-switch bridgeless PFC Dual-Output-Polarities (SSBPFC DOP) converter with a Series-Line-Diode-Clamped (SLDC) configuration, designed to eliminate circulating currents and capacitive coupling loops. The proposed topology addresses critical drawbacks in existing designs, including circulating currents, high maximum current stress on input capacitors and line diodes, and capacitive coupling loops. To overcome these issues, the line diodes are repositioned in series with the input inductors. The converter operates in discontinuous conduction mode (DCM) to achieve a near-unity power factor. The paper thoroughly explains the operational principles and design considerations of the new structure. It also discusses the transition from a two-switch to a single-switch design for both shared and non-shared operation modes. Detailed analyses of circulating current, maximum current stress, and capacitive coupling loop mechanisms are provided. Simulation results demonstrate the complete elimination of circulating currents and capacitive coupling loops, with maximum current stress on input capacitors and line diodes reduced from 13.91 A to 7.6 A.

1. INTRODUCTION

Advancements in power converters have greatly benefited portable electronic devices by providing high efficiency, compact size, and wide input-output voltage flexibility [1]–[3]; however, traditional topologies like buck, boost, buck-boost, and SEPIC-Cuk converters struggle to maintain high efficiency across a broad operating range, especially when both step-up and step-down conversion is required [2], [4], [5]. Additionally, battery voltage decay during discharge poses regulation challenges without proper voltage control [6], making versatile converters like SEPIC and Cuk, which combine step-up and step-down capabilities, valuable for applications in renewable energy, electric vehicles, and consumer electronics [7]–[11].

The SEPIC converter, shown in Figure 1, can step-up or step-down voltage without inverting the output, making it highly adaptable for applications like electric machines, LED systems, solar energy, electric vehicles, and telecommunications [12]–[16]; however, it requires more components, leading to increased size, cost, and potential EMI [17], [18]. In contrast, the Cuk converter, illustrated in Figure 2, also adjusts voltage levels but inverts the output polarity, excelling in energy transfer and managing high input currents while providing smoother energy flow, though at the expense of greater complexity and cost due to additional components [19].

The SEPIC-Cuk converter combines the SEPIC and Cuk converters into a single circuit, delivering continuous current with reduced ripple [20], [21]. This makes it ideal for applications needing stable and efficient power conversion under varying input conditions. Its rising popularity highlights the demand for versatile, high-performance power conversion in today's energy systems. However, the SEPIC-Cuk converter has drawbacks, including higher complexity due to multiple inductors, capacitors, and diodes, which increase cost and size. It may also be less efficient at light lozads compared to simpler

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buck or boost converters and can generate more EMI, requiring extra filtering to meet strict standards.

To address these challenges, the dual-output-polarities (DOP) converter is introduced as an optimized alternative to the SEPIC-Cuk converter. It retains similar capabilities but uses fewer components, reducing cost, size, and footprint. By incorporating a single output diode to manage the current return path, the DOP converter ensures that SEPIC and Cuk outputs have separate grounds, preventing capacitor voltage spikes during energy transfer. Additionally, it employs optimized parameter design to balance energy flow, minimizing noise, spikes, and distortion during operation.

However, some power systems require an AC input source, necessitating rectifiers and DC/DC converters to convert AC to DC based on load needs. However, using a bridge rectifier, transformer, inductor, and capacitor can produce a DC output voltage without distortion but often results in highly distorted input current. Therefore, AC/DC conversion in power factor correction (PFC) converters is critical to ensure that the input voltage and current waveforms remain purely sinusoidal, avoiding dead zones [22], [23]. Dead zones occur when the output full-bridge voltage (V_1) contains excess energy due to an imbalance between the input capacitor (C_1) and output inductor (L_o), leading to distorted input current and a reduced power factor (*PF*). Various topologies, such as boost, buck-boost, SEPIC, and Cuk converters, have been developed for PFC applications [24]–[28].

For example, the conventional PFC SEPIC structure, shown in Figure 3, combines a full-bridge rectifier with a SEPIC converter. This setup often faces power quality issues, including high total harmonic distortion of current (THD_i), low *PF*, dead zones, and significant output voltage ripple [29]–[31]. The full-bridge rectifier's output voltage (V_1) is not a stable DC voltage, so energy must be transferred to the SEPIC efficiently without generating extra energy. Inefficient energy transfer can increase THD_i at the input and worsen output voltage ripple [32].

To address these issues, the conventional bridgeless PFC SEPIC structure, shown in Figure 4, was introduced [33], [34]. However, this design uses two switches, complicating circuit control [35]–[37]. It also suffers from out-of-phase input voltage and current, which lowers the PF. Nonetheless, it requires only one diode rectifier to conduct during positive and negative half-cycles [38].

The existing single-switch bridgeless PFC SEPIC structure, shown in Figure 5, was developed to reduce the number of switches and improve the *PF* [39]. This design ensures that the AC voltage and current sources are in phase. However, it has significant drawbacks, including circulating currents in the input inductors (L_1 and L_2) and high maximum current stress on the line diodes (D_1 and D_2) and input capacitors (C_1 and C_2). These circulating currents occur because diodes D_1 and D_2 are connected to the switch (S), causing the return current path to flow through L_1 and L_2 during both cycles. Besides, capacitive coupling loop occurs at C_1 and C_2.

To overcome these limitations, series-line-diode-clamped (SLDC) configuration is proposed to integrate with DOP converter. This design offers several advantages, including fewer power converters and switches, elimination of circulating currents and capacitive coupling loop, and reduced maximum current stress on line diodes and input capacitors. Additionally, this PFC converter is designed to operate in discontinuous conduction mode (DCM), providing benefits such as zero-current turn-on for the power switch and zero-current turn-off for the output diodes.

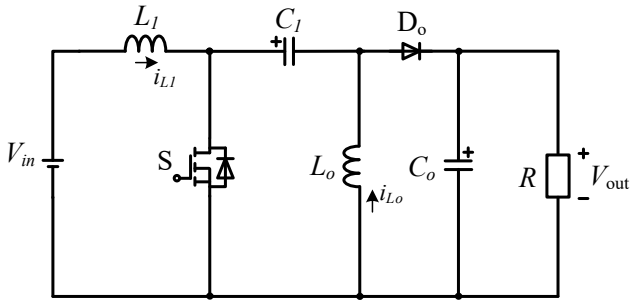


Fig. 1. SEPIC Structure

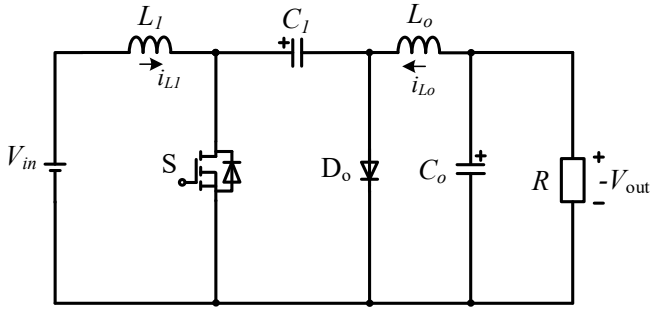


Fig. 2. Cuk Structure

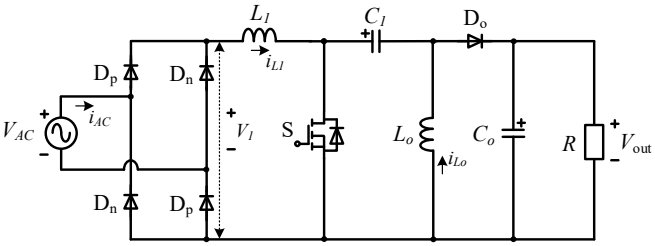


Fig. 3. Conventional PFC SEPIC Structure

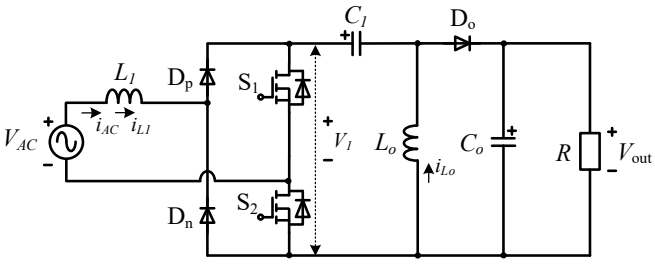


Fig. 4. Conventional Bridgeless PFC SEPIC Structure [33], [34]

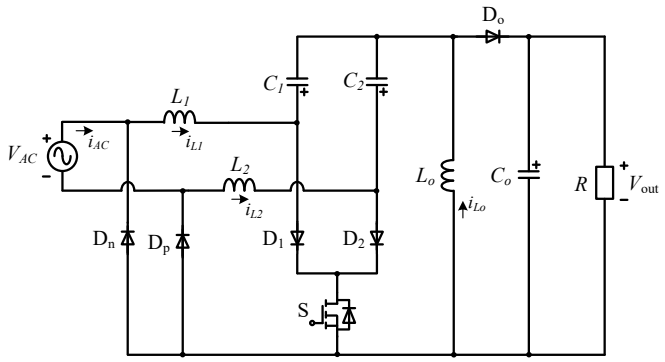


Fig. 5. Existing Single-Switch Bridgeless PFC SEPIC Converter Structure [39]

2. IMPROVEMENTS IN SEPARATED AND SHARED TOPOLOGIES: REDUCING CIRCULATING CURRENTS AND COMPONENT COUNT

This section explores advancements in separated and shared topologies for BPFC SEPIC converters, focusing on their ability to minimize circulating currents and use fewer components. The separated topology tackles circulating currents by employing two input inductors, allowing independent current paths during the positive and negative cycles of the AC source. In contrast, the shared topology simplifies the circuit by reducing the number of output inductors and diodes, but it introduces challenges like capacitive coupling and residual circulating currents. This analysis offers a detailed comparison of both topologies, highlighting their strengths, weaknesses, and potential improvements to boost BPFC SEPIC converter performance.

The separated topology effectively reduces circulating currents by using two input inductors, which support independent operation during the AC source's positive and negative phases. Unlike traditional SEPIC converters that use a single inductor for DC inputs, the BPFC SEPIC design incorporates dual inductors to ensure balanced energy flow and align AC voltage with current phases. While this method improves stability, it increases the number of components and leads to higher conduction losses due to additional inductors and diodes. On the other hand, the shared topology streamlines the circuit by cutting down on output inductors and diodes. However, it faces inefficiencies, such as capacitive coupling loops and circulating currents when the switch is off, as the input capacitors and inductors operate across both cycles. For example, capacitor C_1 works during the positive cycle, while C_2 operates during the negative cycle, and when the switch is off, AC current flows between the inductors, affecting performance. This review emphasizes the trade-offs between the two designs, highlighting the need to balance simplicity and efficiency.

This section evaluates the effectiveness of separated and shared topologies in BPFC SEPIC converters, with a focus on reducing circulating currents and component usage. The separated design successfully eliminates circulating currents by using dual input inductors for independent phase operation, improving energy balance and phase synchronization, though it requires more components and incurs higher losses. Conversely, the shared topology reduces circuit complexity by using fewer output inductors and diodes but struggles with inefficiencies from capacitive coupling and circulating currents due to continuous operation across cycles. Through this comparison, the section sheds light on the balance between minimizing components and maintaining efficiency, providing insights into optimizing BPFC SEPIC converters for specific needs. The findings stress the importance of choosing a topology that aligns with performance goals to achieve an effective balance of simplicity, efficiency, and stability.

2.1 Separated-Operation Designs for Reducing Circulating Currents: Two-Switch BPFC SEPIC Topology

In separated-operation topologies, only the output capacitor and load function jointly, handling current during both positive and negative half-cycles. Other components, however, carry current only during specific cycles. For example, in the positive half-cycle, current flows through L_1, C_1, S_1, L_{o1}, D_{o1}, D_p, while in the negative half-cycle, it passes through L_2, C_2, S_2, L_{o2}, D_{o2}, D_n.

The standard BPFC SEPIC design, known as Structure I [40] and shown in Figure 6, was created to minimize circulating currents at the input inductors. This setup eliminates input switching diodes (D_1 and D_2), using the body diodes of the active switches (S_1 and S_2) to provide a current return path. Without these body diodes, Structure I would not function, as the output inductors (L_o) operate bidirectionally and require a return route for current. However, this design causes a mismatch between AC voltage and current at zero crossing, leading to a lower power factor (*PF*).

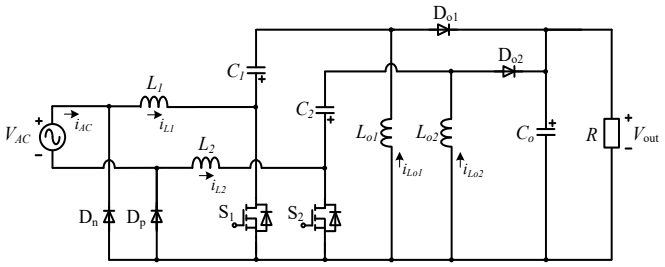


Fig. 6. Structure I [40]

Figure 7 illustrates Structure II, an improved version of Structure I, which adds two input switching diodes (D_1 and D_2) in series with the switches (S_1 and S_2). This setup blocks current flow through the body diodes of the active switches, achieving a near-unity *PF*. However, Structure II has limitations, including circulating currents at the input inductors and increased maximum current stress on the input switching diodes, requiring further improvements.

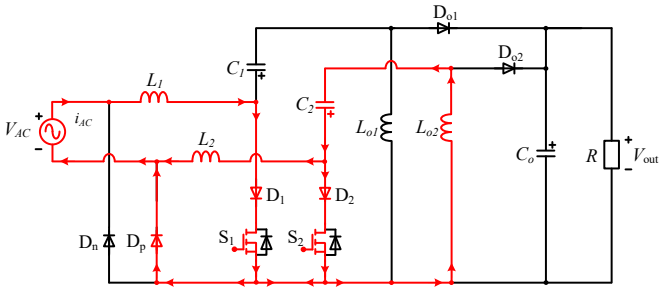


Fig. 7. Structure II (Improved Design to Enhance Structure I)

Structure III, shown in Figure 8, builds on Structure II by placing two input line diodes (D_1 and D_2) in series with the input inductors. This design maintains the *PF* benefit of Structure II

while reducing the maximum current stress on the input line diodes. Nevertheless, it does not eliminate circulating currents at the input inductors and introduces issues like high current stress on the switching diodes and a higher semiconductor count, which increases conduction losses.

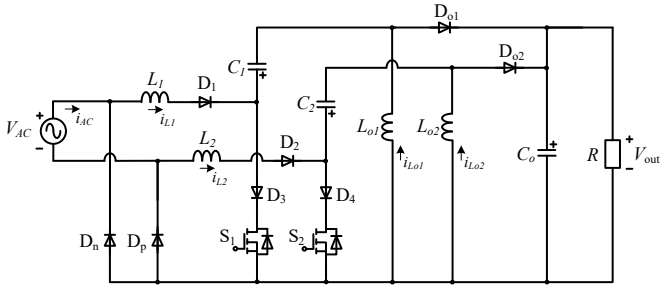


Fig. 8. Structure III (advanced design to improve Structure II)

Figure 9 presents Structure IV, an optimized version of Structure III, achieved by removing the two switching diodes (D_3 and D_4). In this configuration, the input line diodes (D_1 and D_2) are reverse-biased, effectively stopping circulating currents at the input inductors. Additionally, a near-unity *PF* is possible, as each input inductor operates in one direction. Despite these advancements, the practical use of such separated-operation, two-switch topologies is limited by the large number of components and significant conduction losses.

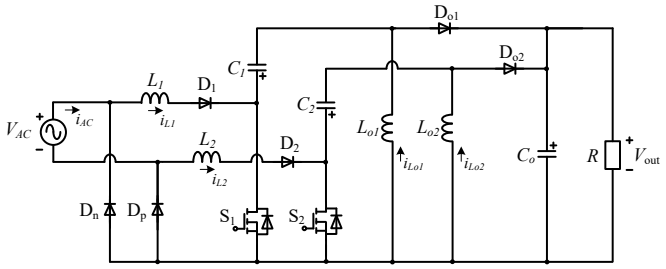


Fig. 9. Structure IV (Optimized Design to Refine Structure III)

2.2 Separated-Operation Designs for Eliminating Circulating Currents: Single-Switch BPFC SEPIC Topology

In separated-operation topologies with a single switch, the number of components is reduced by using only one switch instead of two. This switch operates during both positive and negative half-cycles, simplifying the control of the circuit.

Structure V [41], shown in Figure 10, uses coupled inductors (L_1, L_2, L_3, and L_4) to eliminate circulating currents and reduce noise in current sensing at the low side. This design achieves a near-unity power factor (*PF*) and lowers the number of passive components. By coupling the inductors on a single magnetic core, Structure V reduces both size and cost. However, it has limitations, such as high maximum current stress on the input switching diodes (D_1 and D_2) and the complex design of the coupled inductors. As output power increases, performance decreases due to constraints in the coupled inductor design [42].

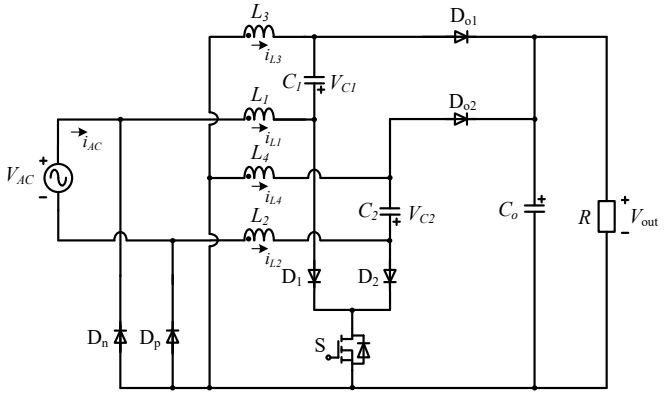


Fig. 10. Structure V [41]

Figure 11 presents Structure VI, an improved version of Structure V, which includes common core inductors (L_1, L_2, L_{o1}, and L_{o2}) and two input switching diodes (D_1 and D_2). This topology retains the benefits and behavior of Structure V. It also allows different inductor values at the input and output within the common core, unlike coupled inductors, which require identical values to maintain volt-microsecond balance. However, using common core inductors does not reduce the number of passive components and still results in high maximum current stress on the input switching diodes.

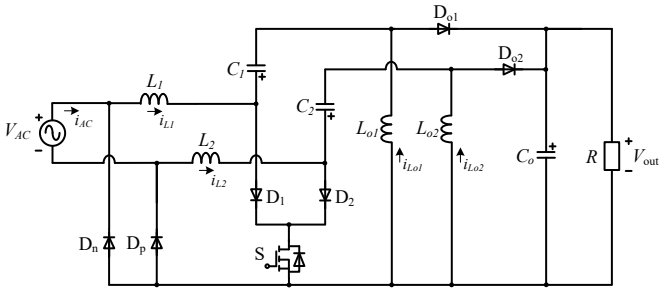


Fig. 11. Structure VI (Improved Design to Enhance Structure V)

Structure VII, illustrated in Figure 12, enhances Structure VI by keeping the common core inductors (L_1, L_2, L_{o1}, and L_{o2}) and replacing the switching diodes with two input line diodes (D_1 and D_2). This design maintains the advantages of Structures V and VI. However, it introduces issues, such as an unwanted capacitive coupling loop between C_1 and C_2 when the switch is off, along with significant current stress on the switch. Overall, single-switch separated-operation topologies do not effectively reduce component count, making them less practical due to increased components and higher conduction losses.

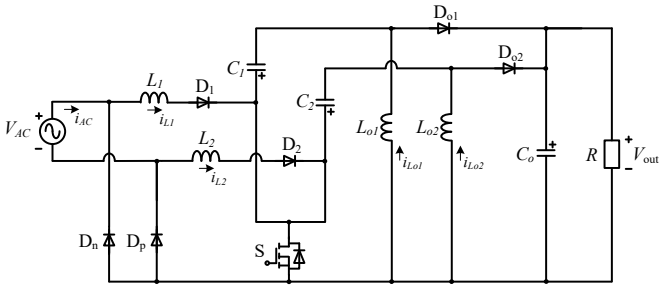


Fig. 12. Structure VII (Advanced Design to Improve Structure VI)

2.3 Shared-Operation Topologies for Reducing Components: Two-Switch BPFC SEPIC Design

In shared-operation topologies, the output inductor, output capacitor, output diode, and load operate together during both positive and negative cycles, with current flowing through these shared components when the circuit is active. Other components, however, conduct current only during specific cycles: for example, L_1, C_1, S_1, and D_p are active in the positive half-cycle, while L_2, C_2, S_2, and D_n are active in the negative half-cycle.

Structure VIII [43], shown in Figure 13, uses a two-switch setup with switches S_1 and S_2, supported by two input switching diodes (D_1 and D_2). A significant advantage of this design is the use of a single control signal for both switches, which simplifies circuit operation. However, it faces several issues, including circulating currents at the input inductors and capacitors, high maximum current stress on the input switching diodes, and a mismatch between AC voltage and current phases, which lowers the power factor (*PF*). Therefore, this topology needs further improvement.

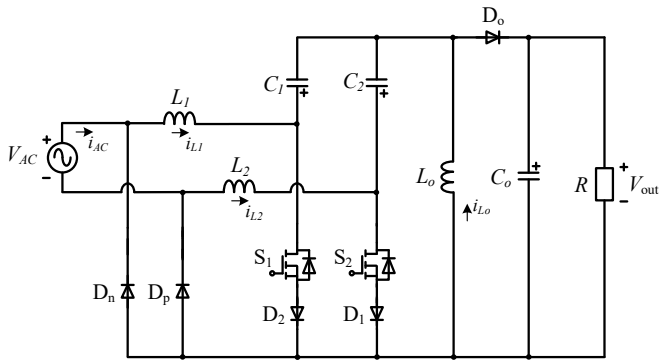


Fig. 13. Structure VIII [43]

Structure IX, illustrated in Figure 14, is an enhanced version of Structure VIII, incorporating two input line diodes (D_1 and D_2). This design achieves a unity *PF* and eliminates circulating currents. However, its practical application is limited due to ongoing capacitive coupling loops and substantial current flow through the input capacitors and MOSFETs. As a result, additional refinements are required for two-switch shared-operation topologies.

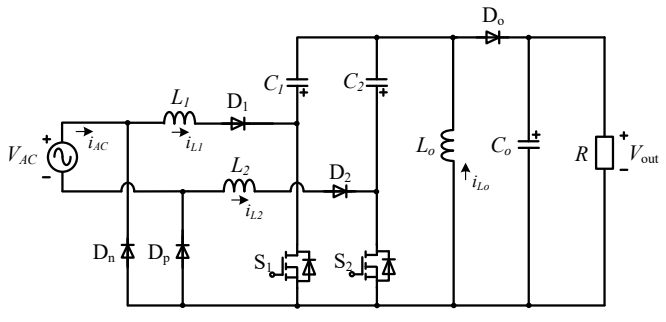


Fig. 14. Structure IX (Refined Design to Improve Structure VIII)

2.4 Shared-Operation Topologies for Reducing Component Count: Single-Switch BPFC SEPIC Design

In shared-operation topologies, a single switch is used to decrease the number of components. This switch operates during both positive and negative half-cycles, simplifying the circuit's control mechanism.

Structure X [39], shown in Figure 15, includes two input switching diodes (D_1 and D_2) and was developed as an improvement over Structure VIII [43]. However, this design has several drawbacks, such as circulating currents between the input inductors (L_1 and L_2) and input capacitors (C_1 and C_2), high maximum current stress on the input switching diodes (D_1 and D_2) and capacitors (C_1 and C_2), and a reduced power factor (*PF*). As a result, further improvements are necessary for this topology.

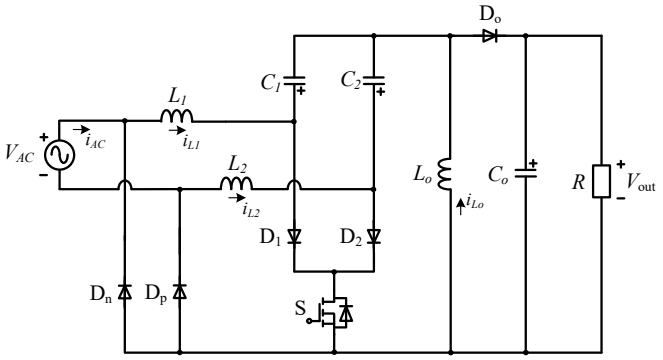


Fig. 15. Structure X [39]

Structure XI, presented in Figure 16, is an enhanced version of Structure X, incorporating two input line diodes (D_1 and D_2). This design overcomes the limitations of Structure X, which provided no significant advantages, by eliminating circulating currents, lowering maximum current stress on the input line diodes (D_1 and D_2) and input capacitors (C_1 and C_2), and achieving a unity *PF*. The reduced stress on the input capacitors (C_1 and C_2) results from their operation across both cycles, despite ongoing capacitive coupling loops. However, additional refinements are needed to make this configuration more compact and simpler.

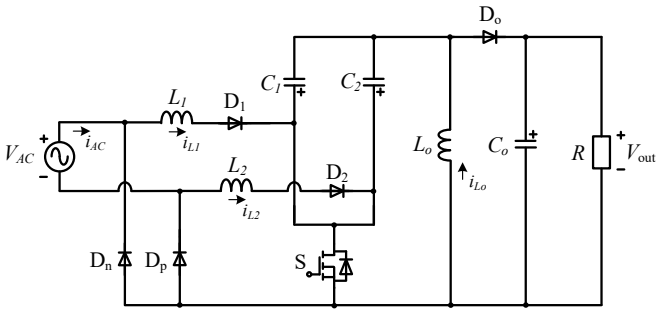


Fig. 16. Structure XI (Proposed Design to Enhance Structure X)

3. Improvements in Separated and Shared Topologies: Reducing Circulating Currents and Component Count

After improving both separated-operation and shared-operation topologies, further refinements were needed to ensure BPFC SEPIC converters could operate with fewer components. Separated-operation designs required more components and led to higher conduction losses, making shared-operation topologies more desirable due to their lower component count.

However, shared-operation designs faced challenges in addressing circulating currents and capacitive coupling loops. Therefore, this study focused on reducing the number of components, eliminating circulating currents and capacitive coupling loops, and lowering maximum current stress on components, aiming to achieve a unity power factor (*PF*) and a simpler circuit design.

3.1 Series-Line-Diode-Clamped (SLDC) Configuration as A Novel Design

The Series-Line-Diode-Clamped (SLDC) configuration was created as a novel topology for various types of DC-DC converters. Shown in Figure 17, this semi-bridgeless SLDC design includes four diodes (D_1, D_2, D_p, and D_n). Traditional BPFC topologies typically use two diodes and two switches, with one pair active during the positive half-cycle and the other during the negative half-cycle. These designs depend on the body diodes of the switches to provide a current return path, required due to the bidirectional operation of the output inductor. In contrast, the semi-bridgeless SLDC places four diodes strategically between the input inductors, eliminating the need for the body diodes of the active switches. Additionally, unlike conventional BPFC designs restricted to MOSFETs, the SLDC topology supports both MOSFETs and IGBTs. The SLDC can be applied to both separated-operation and shared-operation configurations, though separated-operation versions were mainly studied for clarity, despite their higher component count and increased conduction losses. The SLDC design provides multiple advantages, including the elimination of circulating currents, fewer switches and passive components, no reliance on body diodes at active switches, reduced maximum current stress on semiconductors, a unity power factor (*PF*), and a simpler circuit structure.

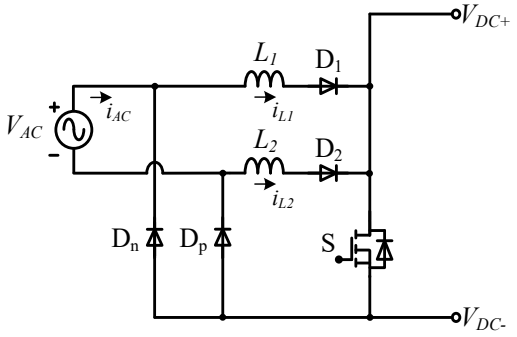


Fig. 17. SLDC as the Improved Proposed Topology

3.2 Principle of BPFC with SLDC Configuration

The Series-Line-Diode-Clamped (SLDC) configuration for the bridgeless power factor correction (BPFC) topology, shown in Figure 18, includes four standard diodes, two inductors, and a single MOSFET. A key benefit of this design is the use of only one switch to control the circuit during both positive and negative half-cycles.

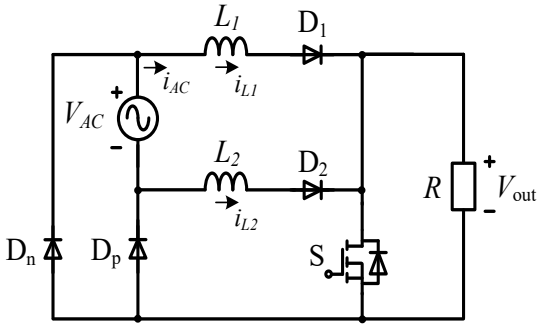


Fig. 18. SLDC Configuration for BPFC Topology

The chopped DC voltage output is created by the MOSFET's switching, controlled by the duty cycle, alternating between on and off states. The line diodes operate in forward-biased mode, guiding current through different paths during the positive and negative half-cycles, as illustrated in Figure 19. Two inductors help produce the chopped DC output and maintain energy balance between the half-cycles. As a result, this topology achieves a near-unity power factor (*PF*), with voltage and current aligned at the zero-crossing point.

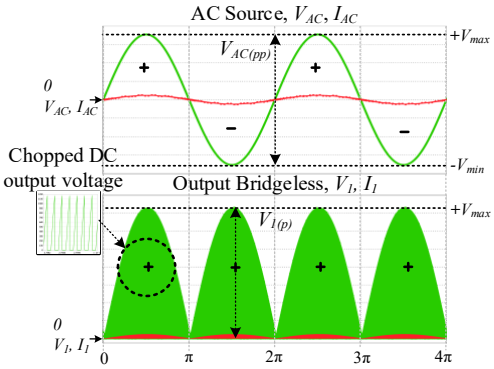


Fig. 19. AC Source and Chopped DC Output Voltage

Positive Half-Cycle: In the positive half-cycle, when the switch (S) is on, diodes D_1 and D_p conduct in series, while diodes D_2 and D_n remain reverse-biased, allowing the input inductor (L_1) to charge. When the switch is off, diodes D_1 and D_p continue to conduct, with D_2 and D_n still reverse-biased. The inductor L_1 discharges, sending current through the load, resulting in a chopped DC voltage output during this phase.

Negative Half-Cycle: In the negative half-cycle, when the switch (S) is on, diodes D_2 and D_n conduct in series, while diodes D_1 and D_p are reverse-biased, charging the input inductor (L_2). When the switch is off, diodes D_2 and D_n continue conducting, with D_1 and D_p remaining reverse-biased. The inductor L_2 discharges, directing current through the load, producing a chopped DC voltage output during this phase.

3.3 Single-Switch Bridgeless PFC DOP Converter with SLDC Configuration

The SLDC configuration for BPFC SEPIC converters was designed to reduce component count and eliminate circulating currents. However, shared-operation topologies using this configuration still faced issues with capacitive coupling loops between input capacitors, as these capacitors operate during both positive and negative half-cycles. By using a single input capacitor that functions across both cycles, the maximum

current stress on the capacitor remained similar to that seen in the earlier Structure X.

Figure 20 shows Structure XII, a Two-Switch Bridgeless PFC (TSBPFC) SEPIC with SLDC configuration, featuring a single input capacitor (C_1) and two switches (S_1 and S_2). This design provides several benefits, including lower maximum current stress on semiconductors and switches, while achieving a unity power factor (*PF*). However, using two switches makes the circuit control more complex.

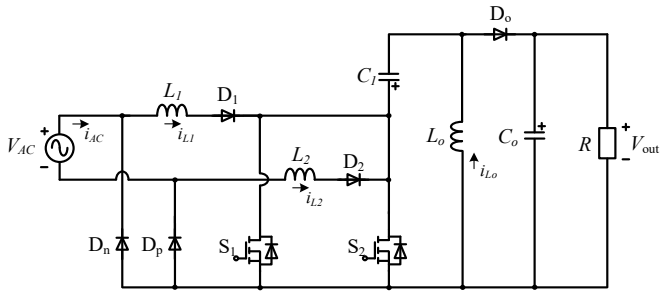


Fig. 20. Structure XII (Two-Switch Bridgeless PFC SEPIC with SLDC Topology)

Figure 21 introduces Structure XIII, an improved design over previous topologies, configured as a Single-Switch Bridgeless PFC (SSBPFC) SEPIC with SLDC topology. This structure uses a single switch (S_1) and fewer components, eliminating circulating currents and capacitive coupling loops, reducing the number of switches and input capacitors, and lowering maximum current stress on semiconductors. It also achieves a unity *PF*, offers a simpler design, and reduces both cost and size.

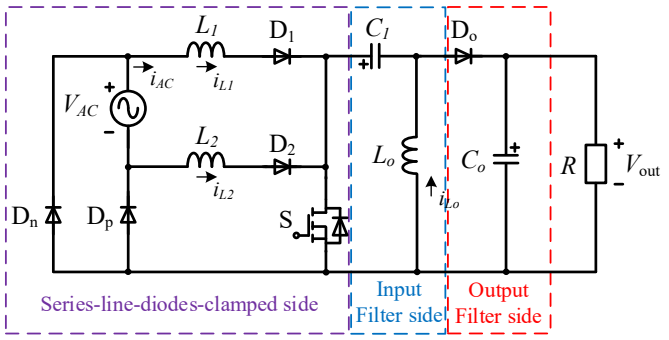


Fig. 21. Structure XIII (Single-Switch Bridgeless PFC SEPIC with SLDC Topology)

Besides, to verify the robustness of SLDC configuration topology, the SLDC configuration also can integrate with dual-output-polarities (DOP) converter as shown in Figure 22. The DOP converter integrates the benefits of SEPIC and Cuk converters, offering improved current handling, lower voltage stress on components, wider input and output voltage ranges, and flexible output polarities. It provides versatile voltage conversion, capable of both stepping up and stepping down voltages, making it suitable for applications where the input voltage fluctuates or must be adjusted to meet load requirements. The DOP converter is designed to function effectively across a broad range of input and output voltages, making it ideal for systems with variable input sources or specific output voltage needs. Furthermore, it is well-suited for energy storage applications requiring bidirectional energy flow, enabling efficient charging and discharging of energy storage components.

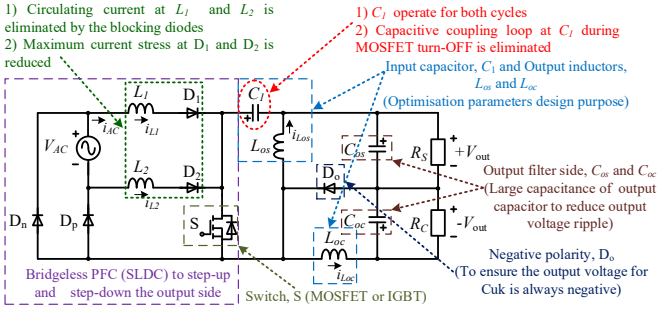


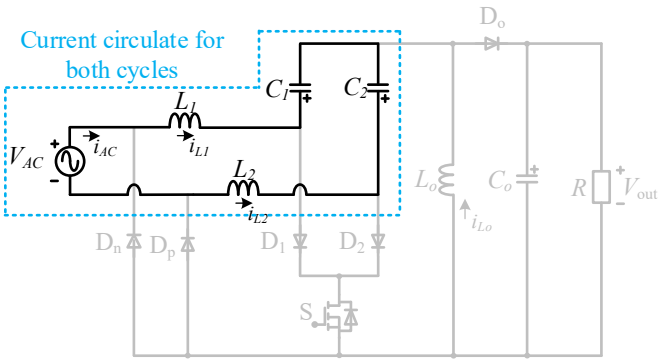
Fig. 22. Proposed Single-Switch Bridgeless PFC DOP Converter with SLDC Configuration

The issues of circulating currents, capacitive coupling loops, and high maximum current stress on components are analyzed in this study, supported by theoretical analyses and simulation results.

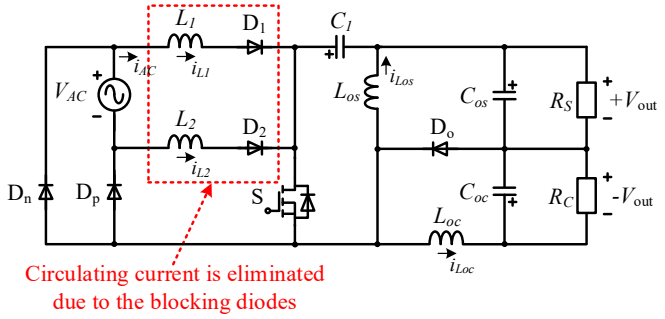
3.4 Principle of Circulating Current Elimination

Figure 23 compares the diode arrangements in Structure X and the Single-Switch Bridgeless Power Factor Correction (SSBPFC) Dual-Output-Polarities (DOP) topology with Series-Line-Diode-Clamped (SLDC) configuration. In Structure X, shown in Figure 23 (a), diodes D_1 and D_2 are placed in series with the MOSFET S. When S is turned on, input inductors L_1 and L_2 store energy from the AC source, but a circulating current develops between L_1 and L_2 during the charging phase. When S is turned off, diodes D_1 and D_2 stop conducting, and L_1 and L_2 discharge, yet the circulating current between L_1 and L_2 persists. This circulating current occurs in both positive and negative half-cycles, during both switch-on and switch-off states. Ideally, L_1 and L_2 should function only during their respective half-cycles to maintain discontinuous conduction mode (DCM), based on the current flow through the input inductors.

The SLDC configuration, illustrated in Figure 23 (b), is designed to eliminate circulating currents in L_1 and L_2 during positive and negative half-cycles. In the positive half-cycle, when MOSFET S is on, the AC current flows through L_1, while diode D_2 blocks current, isolating L_2. When S is off, the inductor current flows directly to capacitor C_1, with D_2 remaining non-conductive, preventing circulating current in L_2. Similarly, during the negative half-cycle, the same mechanism suppresses circulating current in L_1, as shown in Figure 23 (b).



(a)

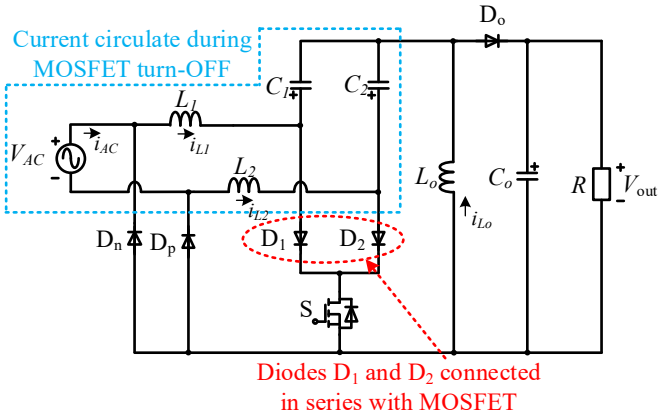


(b)

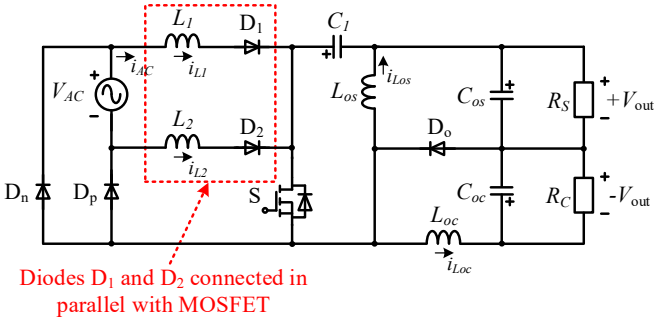
Fig. 23. Diode Placement Comparison: (a) Structure X, (b) SSBPFC DOP Topology with SLDC Configuration

3.5 Impact of Maximum Current Stress Reduction at Line Diodes

The maximum current stress on diodes is determined based on their operating modes. Unlike power loss, which builds up over time, maximum current stress represents the peak current flowing through the diodes at specific moments, particularly at line frequency angles of π/2 and 3π/2 within a single cycle. Therefore, choosing the appropriate diodes depends on these peak current values. In Structure X, shown in Figure 24 (a), the maximum current stress on input diodes D_1 and D_2 matches that on the MOSFET S because they are connected in series. In contrast, the SSBPFC DOP with SLDC configuration, illustrated in Figure 24 (b), has maximum current stress on line diodes D_1 and D_2 equal to that on input inductors L_1 and L_2. In both topologies, the input and line diodes operate during distinct half-cycles. A major benefit of the SLDC configuration is the reduced maximum current stress on D_1 and D_2. Additionally, the SSBPFC DOP with SLDC configuration allows the use of either standard or fast-recovery diodes, while Structure X requires fast-recovery diodes only.



(a)

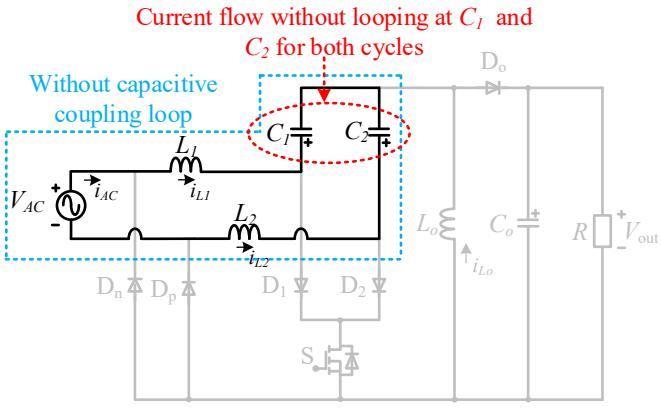


(b)

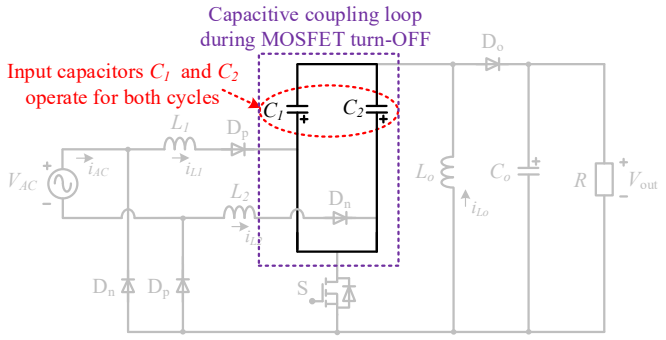
Fig. 24. Maximum Current Stress on Diodes: (a) Structure X, (b) SSBPFC DOP Topology with SLDC Configuration

3.6 Principles of Capacitive Coupling Loop and Maximum Current Stress Reduction at Input Capacitors

Figure 25 shows the circulating and looping currents impacting input capacitors C_1 and C_2 in Structure X and Structure XI. Circulating current, different from looping current, refers to the current from the AC source flowing through C_1 and C_2, as illustrated in Figure 25 (a). Looping current, on the other hand, occurs when current flows between C_1 and C_2 from the AC source during the MOSFET (S) off state, as depicted in Figure 25 (b). In Structure X's diode-clamped configuration, circulating currents are prominent in C_1 and C_2. In contrast, the Series-Line-Diode-Clamped (SLDC) configuration in Structure XI creates a looping current between C_1 and C_2, significantly reducing the maximum current stress on these capacitors. When capacitors are connected in parallel, the current splits between them, cutting the stress on each capacitor in half. In a series connection, however, the current through each capacitor remains the same. Thus, the parallel configuration in Structure XI greatly reduces the maximum current stress on C_1 and C_2.



(a)

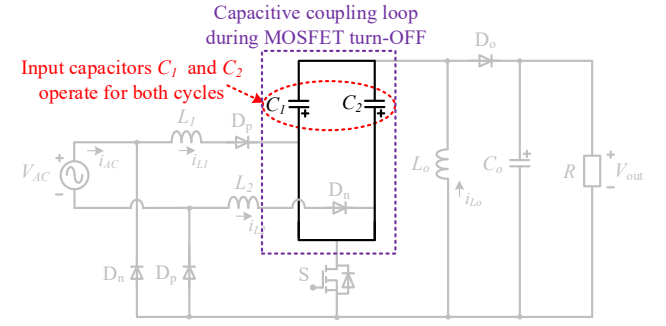


(b)

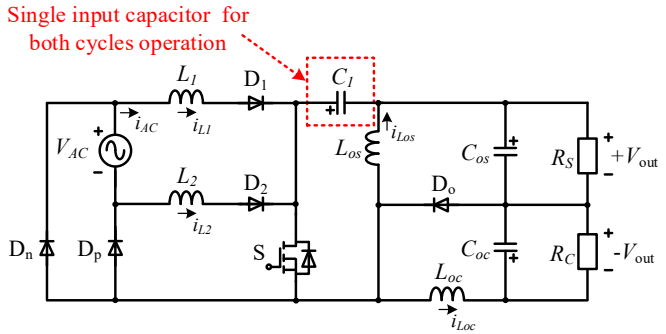
Fig. 25. Circulating and Looping Current Paths at Input Capacitors: (a) Structure X, (b) Structure XI

3.7 Elimination of Capacitive Coupling Loop at Input Capacitors

Reducing the number of input capacitors can help eliminate the capacitive coupling loop. Figure 26 shows how the SLDC configuration addresses this issue by using fewer input capacitors. In Structure XI, shown in Figure 26 (a), the SLDC configuration creates a capacitive coupling loop during both positive and negative half-cycles, which reduces the maximum current stress on input capacitors. However, by using a single input capacitor in the SLDC configuration, as illustrated in Figure 26 (b), the SSBPFC DOP topology completely eliminates the capacitive coupling loop. This reduction does not further lower the maximum current stress on the input capacitor, which remains similar to that in Structure X. Nonetheless, the single input capacitor functions across both half-cycles, improving the efficiency of the circuit.



(a)



(b)

Fig. 26. Input Capacitor Reduction for Eliminating Capacitive Coupling Loop: (a) Structure XI, (b) SSBPFC DOP Topology with SLDC Configuration

4. PARAMETER DESIGN

Table 1 provides the specifications for designing the passive components, including capacitors and inductors. The values of these components are calculated based on the discontinuous conduction mode (DCM) condition, as outlined in references [5][39].

Table 1. Specifications

Parameters	Values
Input voltage, V_{AC}	(50-100) V
Frequency line, f_L	50 Hz
Period of line voltage, T_L	0.02 s
Output voltage (DC), $\pm V_{out}$	±48 V
Output power, P_{out}	160 W
Switching frequency, f_s	50 kHz
Maximum input current ripple, Δi_{L1}	< 25% of fundamental current
Output voltage ripple, ΔV_o	< 5% of V_o

4.1 Determination of Input Inductor

The input inductors (L_1 and L_2) are determined using (1), based on the input voltage (V_{AC}) during the positive and negative half-cycles.

$$L_1 = L_2 = \frac{V_{AC}(t)\cdot D_1}{\Delta I_{Lx}\cdot f_s} \tag{1}$$

$$L_x = L_1 = L_2 \tag{2}$$

4.2 Determination of Output Inductor

The voltage conversion ratio M, derived from the rectifier parameters, is calculated using the power balance principle [44]:

$$M = \frac{V_o}{\sqrt{2}\times V_{AC}} \tag{3}$$

The value of $K_{e\text{-}critical}$ can be evaluated from:

$$K_e < K_{e-critical} = \frac{1}{2(M+2)^2} \tag{4}$$

In order to ensure the operation is in DCM, the following value of K_e is selected:

$$K_e = 0.85\times K_{e-critical} \tag{5}$$

Thus, evaluating parameter K_e gives an equivalent inductance L_e value of:

$$L_e = \frac{K_e\cdot R_L}{2\cdot f_s} \tag{6}$$

The value of L_o can be expressed as follows:

$$L_o = \frac{2L_x\cdot L_e}{L_x - L_e} \tag{7}$$

$$L_o = L_{os} = L_{oc} \tag{8}$$

4.3 Determination of Input Capacitor

The input capacitors C_1 and C_2 are designed to prevent low-frequency oscillations with the converter inductors. Their

energy transfer is based on inductors L_1, L_2, and L_o, ensuring the line frequency (f_L) is much lower than the switching frequency (f_s). A good starting point for selecting the resonant frequency (f_r) is given by [5]:

$$f_L < f_r < f_s \tag{9}$$

$$f_r = \frac{1}{2\pi\sqrt{C_x(L_x + L_o)}} \tag{10}$$

$$C_x = C_1 = C_2 \tag{11}$$

4.4 Determination of Output Capacitor

The output voltage ripple frequency of the converter is twice the input frequency. Thus, the output capacitor C_o is determined as follows:

$$C_o = \frac{P_o}{4 f_L \cdot V_o \cdot \Delta V_o} \tag{12}$$

$$C_o = C_{os} = C_{oc} \tag{13}$$

By considering the availability of components in the market, the specifications for the modified single-switch bridgeless PFC SEPIC structure are presented in Table 2.

Table 2. Design Parameters for Passive Components

Parameters	Values
Input inductors, L_x (L_1= L_2)	2.2 mH
Output Inductor, L_o	22 µH
Input capacitors, C_x (C_1= C_2)	1 µF
Output Capacitor, C_o	3300 µF

5. Simulation Results And Discussion

This section discusses simulation results for elimination of circulating current and capacitive coupling loop, and reduction of maximum current stress at line diodes and input capacitors.

5.1 Simulation Results Showing Elimination of Circulating Current

The Figure 27 presents simulation results comparing the input inductors L_1 and L_2 in Structure X and the SSBPFC DOP with SLDC configuration. In Structure X, circulating currents appear in both L_1 and L_2 during positive and negative half-cycles. For analysis, we focus on the circulating current in L_1 across both cycles under ideal conditions. In contrast, the SSBPFC DOP with SLDC configuration shows no circulating currents in the input inductors.

During the positive half-cycle, the peak current in L_1 for Structure X reaches 3.05 A, while it is only 2.75 A for the SSBPFC DOP with SLDC configuration. In Structure X, a circulating current persists in the negative half-cycle, with an inductor current ripple of 0.25 A, whereas the SSBPFC DOP with SLDC configuration has zero ripple (0 A). The ripple in L_1 during the negative half-cycle in Structure X matches the positive half-cycle's ripple at peak times. This ripple occurs because the AC source draws energy, forcing L_1 to remain active during the negative half-cycle. These circulating current losses act as an energy buffer in the negative half-cycle.

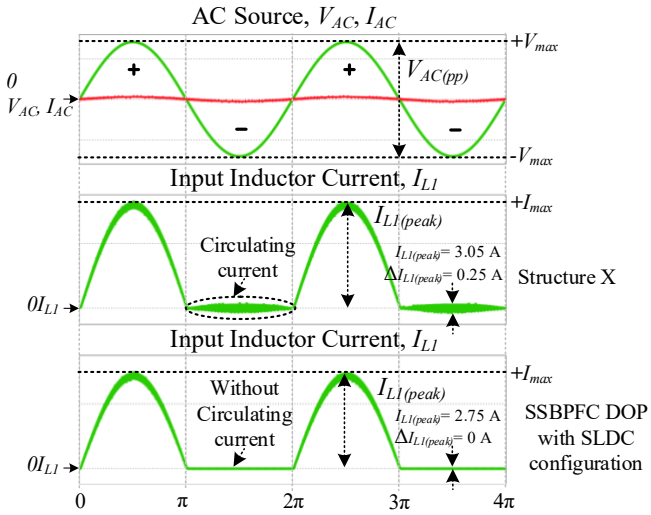


Fig. 27. Simulated Current in Input Inductor, L_1 for Structure X and SSBPFC DOP Topology with SLDC Configuration

5.2 Simulation Results for Reduced Maximum Current Stress on Line Diodes D_1 and D_2

Simulation results, shown in Figure 28, compare the maximum current stress on line diodes in Structure X and the SSBPFC DOP with SLDC configuration. The analysis focuses on diode D_1 for both topologies, as D_2 exhibits identical behavior. In Structure X, the peak current through input diode D_1, $I_{D1(peak)}$, reaches 14.25 A at a 50 kHz switching frequency, resulting in a chopped DC current due to switching. In contrast, the SSBPFC DOP with SLDC configuration shows a much lower peak I_{D1} of 2.98 A at a 50 Hz line frequency. In the SLDC configuration, the current through the line diodes is unaffected by the switching frequency because the MOSFET is connected in parallel, making the current through D_1 equal to that of input inductor L_1. The results for D_2 are the same as those for D_1 in both topologies.

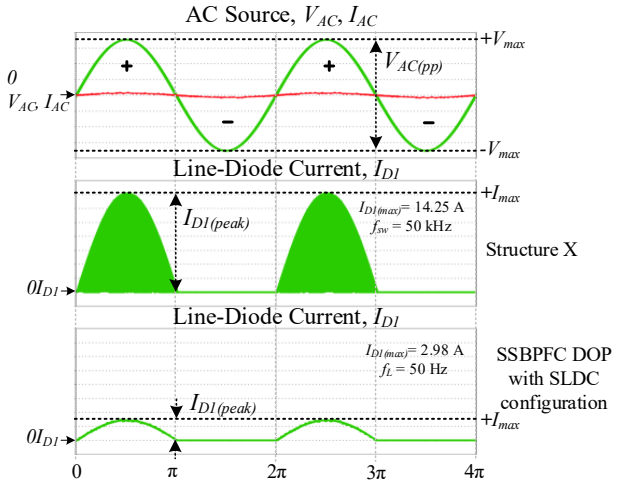


Fig. 28. Simulated Maximum Current Stress on Line Diodes for Structure X and SSBPFC DOP Topology with SLDC Configuration

5.3 Simulation Results for Reduced Maximum Current Stress at Input Capacitors

Figure 29 shows simulation results comparing the current stress on input capacitors in Structure X and Structure XI. The analysis focuses on the maximum current stress at input capacitor C_1 for both topologies, as C_2 exhibits the same behavior as C_1. In Structure X, simulations show a peak-to-peak current, $I_{C1(pp)}$, of 13.91 A. In contrast, Structure XI has a lower $I_{C1(pp)}$ of 7.6 A. In Structure X, C_1 operates only during one half-cycle, while in Structure XI, C_1 functions during both positive and negative half-cycles, resulting in a current through C_1 that is roughly half that of Structure X. This reduction occurs due to a looping current caused by the blocking action of line diodes D_1 and D_2 in Structure XI. These diodes enable a parallel connection of capacitors, splitting the current through C_1 into two paths during both cycles, a phenomenon known as the capacitive coupling loop. In Structure X, a series connection causes identical currents through C_1 and C_2, with each capacitor active in only one half-cycle. The results for C_2 are the same as those for C_1 in both topologies.

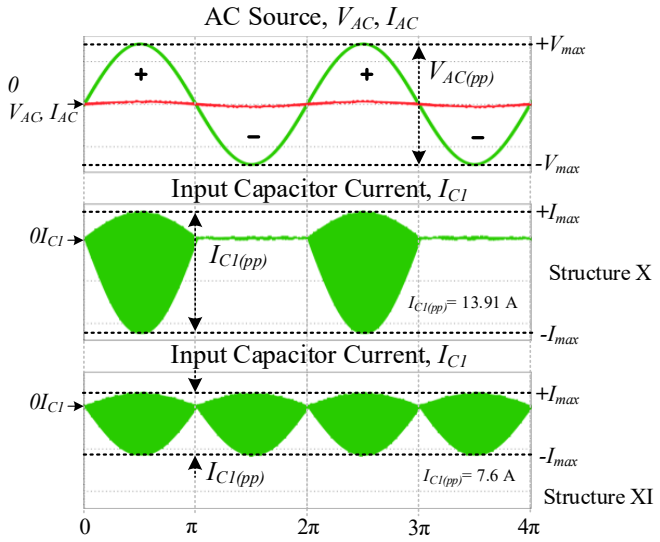


Fig. 29. Simulated Current Stress at Input Capacitors for Structure X and Structure XI

5.4 Simulation Results for Elimination of Capacitive Coupling Loop at Input Capacitors

Figure 30 shows simulation results illustrating the elimination of the capacitive coupling loop at the input capacitor by reducing the number of capacitors. The analysis examines the maximum current stress on input capacitor C_1 in Structure XI and the SSBPFC DOP with SLDC configuration. Simulations indicate that Structure XI has a maximum current stress on C_1 of 7.6 A, while the SSBPFC DOP with SLDC configuration shows 13.91 A, matching the value observed in Structure X. The key difference is that C_1 in the SSBPFC DOP with SLDC configuration operates during both positive and negative half-cycles, unlike Structure X, where C_1 is active only in one half-cycle. By using a single input capacitor in the SSBPFC DOP with SLDC configuration, C_1 functions across both cycles, completely eliminating the capacitive coupling loop when the MOSFET (S) is off.

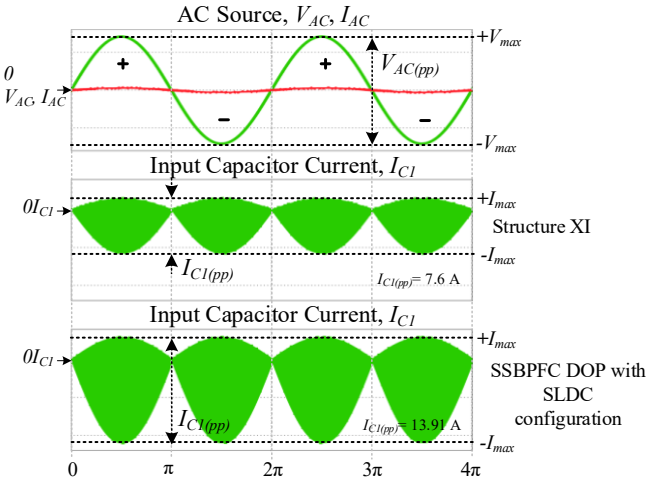


Fig. 30. Simulated Elimination of Capacitive Coupling Loop at Input Capacitor through Reduced Capacitor Count

6. CONCLUSION

This paper introduces a novel single-switch bridgeless PFC Dual-Output-Polarities (SSBPFC DOP) converter with a Series-Line-Diode-Clamped (SLDC) configuration, designed with fewer components for simplicity. The simulation results align closely with the intended design specifications. Simulations confirm the complete elimination of circulating currents, reducing from 0.25 A to 0 A, and the removal of capacitive coupling loops. Additionally, the maximum current stress on input capacitors is reduced from 13.91 A to 7.6 A, and on-line diodes from 14.25 A to 2.98 A. The converter achieved unity *PF*.

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